Amendments to the Specification:

Please replace the paragraph [004] with the following paragraph:

After prelayout simulation 24 is satisfactory, a layout tool ~~35~~ 25 is used to create physical layout of the design begining with floorplanning in step 26 in which the blocks of the netlist 20 are arranged on the chip. The location of the cells in the blocks are then determined during a placement process in step 28. A routing process makes connections between cells and blocks in step 30. Thereafter, circuit extraction determines the resistance and capacitance of the interconnects in step 32. A postlayout simulation is then performed in step 34 from which the overall timing and performance of the chip can be determined, with successive refinement to floorplanning 26 as necessary.

Please replace the paragraph [009] with the following paragraph:

The present invention provides a method and system for optimizing a netlist change order flow is disclosed, wherein a design layout created by a layout tool using a reference netlist is to be changed by a modified version of the netlist, and wherein both ~~netlist~~ netlists are hierarchical comprising. Aspects of the present invention include comparing the modified netlist with the original netlist outside of the layout tool, and automatically generating at least one change order based on differences found between the two netlists. After the change order is generated, the change order is then applied to the design layout to generate a modified design layout.